Docket No.: 64965-122

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Jeffrey DWORK	:	Confirmation Number: 5577
Application No.: 09/481,388	:	Tech Center Art Unit: 2182
Filed: January 12, 2000	:	Examiner: N. Patel
For: ALTERNATE REGISTER MAPPING	:	

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is Appellant's Appeal Brief in support of the Notice of Appeal filed August 23, 2004. Please charge the Appeal Brief fee of $340.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due under 37 C.F.R. and 41.20, and in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed August 23, 2004, wherein Appellant appeals from the Primary Examiner's rejection.

Real Party In Interest

This application is assigned to Advanced Micro Devices, Inc. by assignment recorded on January 12, 2000, at Reel 010490, Frame 0277.

Related Appeals and Interferences

No other appeals or interferences are known to the Appellant, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Status of Claims

Claims 1-13 and 15-20 are pending. Claim 14 is cancelled. Claims 1-13 and 15-20 stand under final rejection, from which rejection this appeal is taken.

Status of Amendments

The application has not been amended after final Office Action.

Summary of Claimed Subject Matter

Software for managing communications between a CPU and network devices may require that certain bits in a network device, such as control and status bits, be accessed in a specific way. For example, a particular bit is required to be located in a specific position in a particular register along with some other bits accessible during the same access operation or sequence of access operations.

Thus, to be able to operate with different types of software, a network device should store the same information in various registers. Separate control means should be provided to maintain consistency of bits corresponding to the same information.

The present invention enables a network device to operate with different types of software without storing the same information in different locations. As shown in Figure 2 of the present application, a network interface 10 comprises a register logic block 100 that manages top-level registers of the network interface 10. The register logic block 100 is coupled to the PCI bus interface unit 16 via a register interface 102 to allow read and write accesses to the registers.

For example, the register logic block 100 may include a decoder and multiple global registers such as control and status registers, and interrupt registers. The control and status registers may comprise control bits for controlling some functions of the network interface 10 such as switching into

a particular mode of operation, the start or stop of frame transmission or reception, and status bits for indicating the status of certain network interface operations. The interrupt registers may comprise interrupt bits corresponding to various transmit and receive interrupt events.

The register logic block 100 comprises alternate register access circuitry 110 for providing alternate access to certain bits stored in registers of the register logic block 100. Figure 3 of the application illustrates an exemplary alternate register access circuitry 110 for providing read and write accesses to a storage element 120, such as a flip-flop, that holds the value of a control bit F1. The control bit F1 may be a bit set or cleared by a PCI write access, and used to control some function within the network interface 10. For example, the control bit F1 may be set to instruct the network interface 10 to switch into a particular mode of operation, to start or stop frame transmission or reception, etc.

The storage element 120 for holding the bit F1 can be accessed in two different ways. First, it can be accessed as a bit arranged in a first register such as register 3, in a first bit position, for example, position 1 of the register 3. Also, this storage element can be accessed as a bit arranged in a second register such as register 8, in a second bit position, for example, position 5 of the register 8. As a result, the bit F1 can be written or read to or from a single storage element when the network interface 10 is controlled by a first type of software that requires this bit to be in the first register, and when the network interface 10 is controlled by a second type of software that requires the bit F1 to be arranged in the second register.

When the network interface 20 is controlled by the first type of software to write data into the memory element 120, a register address signal identifying the register 3, together with the write signal, is supplied to the register logic block 100. When the network interface 20 is controlled by the second

type of software to write data into the memory element 120, a register address signal identifying the register 8, together with the write signal, is supplied to the register logic block 100.

When the network interface 10 operates with the first type of software, a read access operation to bit position 1 of the register 3 results in reading the control bit F1 from the storage element 120 as the DATA[1] signal. Similarly, when the network interface 10 operates with the second type of software, a read access operation to bit position 5 of the register 8 results in reading the control bit F1 from the storage element 120 as the DATA[5] signal.

Accordingly, the present invention enables the network interface 10 to operate with different types of software without storing the same information in different locations. Instead, a particular bit accessible via the PCI bus is stored in a single storage element. Alternate register access circuitry provides alternate circuits for accessing this storage element. When the network interface operates with a first type of software, the storage element is being accessed as a first position of a first register. However, when the network interface operates with a second type of software, the storage element is being accessed as a second position of a second register.

Grounds of Rejection To Be Reviewed By Appeal

Whether claims 1-13 and 15-20 are unpatentable over Watkins in view of Hansen under 35 U.S.C. § 103.

Argument

In the application of a rejection under 35 U.S.C. §103, it is incumbent upon the Examiner to factually support a conclusion of obviousness. As stated in ***Graham v. John Deere Co.*** 383 U.S. 1, 13, 148 U.S.P.Q. 459, 465 (1966), obviousness under 35 U.S.C. §103 must be determined by considering

(1) the scope and content of the prior art; (2) ascertaining the differences between the prior art and the claims in issue; and (3) resolving the level of ordinary skill in the pertinent art.

As demonstrated below, the Examiner has failed to factually support his conclusion of obviousness.

Claims 1-13

Claim 1 recites a data processing system operable with at least two types of software. The system comprises:

- a host interface for providing address, data and control signals from a host,

- a storage element for holding data accessible via the host interface, and

- alternate access circuitry for providing access to the storage element so as to access the data as a first data element in a first register when the system operates with a first type of software, and as a second data element in a second register when the system operates with a second type of software.

Hence, claim 1 requires accessing the data held in the storage element as a first data element in a first register when the system operates with a first type of software, and accessing the same data as a second data element in a second register when the system operates with a second type of software.

The Examiner holds Watkins to differ from the claimed invention only in that the reference does not disclose the claimed alternate access circuitry for providing access to the storage element so as to access the data as a first data element in a first register when the system operates with a first type of software, and as a second data element in a second register when the system operates with a second type of software.

Hansen is relied upon for disclosing the alternate access circuitry. In particular, in his Response to the Applicant's Arguments, the Examiner relies upon col. 15, lines 29-46 of Hansen.

Considering the reference, Hansen describes a virtual memory system that translates a task specific virtual address into a generalized virtual address, and translates the generalized virtual address into a physical address (col. 2, lines 45-51, col. 4, lines 45-57). The system has multiple simultaneous threads of execution. Each of the threads corresponds to different independent tasks. Data may be shared or maintained independently between each thread "since each thread has a distinct version of the local translation look-aside buffer (TLB) so that they may use the same address to mean different things, or may use the same address to reference the same memory" (col. 15, lines 29-46).

The reference does not disclose or suggest that "the same address meaning different things" corresponds to the claimed storage element storing data accessed as a first data element in a first register when the system operates with a first type of software, and as a second data element in a second register when the system operates with a second type of software, as claim 1 requires.

Hence, the reference does not disclose the alternate access circuitry for providing access to the storage element so as to access the data as a first data element in a first register when the system operates with a first type of software, and as a second data element in a second register when the system operates with a second type of software, as claim 1 requires.

Moreover, one skilled in the art would recognize that the term "thread" relates to portions of the same program that can run independently and concurrently. Therefore, multiple threads of execution

described in the Hansen patent are executed when the Hansen system operates with the same software rather than with different types of software, as claim 1 requires.

In the Advisory Action, the Examiner relies upon the definition of the term "software" as "instructions that make hardware work." Accordingly, it appears that the Examiner interprets different threads as different types of software. The Examiner's position is respectfully traversed.

Hansen provides no reason to conclude that different threads involve different types of instructions. By contrast, each thread relates to the same program. Therefore, they involve the same type of instructions. Accordingly, different threads are software of the same type, rather than software of different types.

Moreover, even assuming *arguendo* that the threads are software of different types, Hansen does not disclose providing access to the storage element so as to access the same data as different elements in different registers when the system operates with different threads.

It is respectfully submitted that the phrase "since each thread has a distinct version of the local translation look-aside buffer (TLB) so that they may use the same address to mean different things, or may use the same address to reference the same memory" relied upon by the Examiner provides no reason to conclude that the system provides access to the same data as different elements in different registers when the system operates with different threads.

One skilled in the art would understand that in the Hansen virtual memory system that translates a task specific virtual address into a generalized virtual address, and translates the generalized virtual address into a physical address, the phrase "the same address meaning different

things" may relate to correspondence between physical and virtual addresses, and imply that the same virtual address may correspond to different physical addresses or to the same physical address.

Accordingly, Hansen does not disclose accessing the data held in the storage element as a first data element in a first register when the system operates with a first type of software, and accessing the same data as a second data element in a second register when the system operates with a second type of software.

Therefore, neither Watkins nor Hansen discloses the claimed alternate access circuitry for providing access to the storage element so as to access the data as a first data element in a first register when the system operates with a first type of software, and as a second data element in a second register when the system operates with a second type of software.

It is well settled that the test for obviousness is what the combined teachings of the references would have suggested to those having ordinary skill in the art. ***Cable Electric Products, Inc. v. Genmark, Inc.***, 770 F.2d 1015, 226 USPQ 881 (Fed. Cir. 1985). In determining whether a case of prima facie obviousness exists, it is necessary to ascertain whether the prior art teachings appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification. ***In re Lalu***, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

As demonstrated above, the combination of references applied by the Examiner is not sufficient to arrive at the claimed alternate access circuitry. Therefore, the Examiner's conclusion of obviousness is not warranted.

Further, the Examiner must provide a reason why one having ordinary skill in the art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. ***Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.***, 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985). ***In re Fine***, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); ***Stratoflex, Inc. v. Aeroquip Corp.***, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); ***In re Warner***, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967).

These showings by the Examiner are an essential part of complying with the burden of presenting a *prima facie* case of obviousness. ***In re Oetiker***, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

The Examiner takes the position that it would have been obvious to incorporate the Hansen's system into the Watkins' system to "allow multiple programs to simultaneously share a computer system's main memory and increase the overall efficiency and flexibility of the system."

Watkins discloses multiple microprocessors 210 sharing main memory 220 that includes buffers consequently addressed in virtual memory. The address translation unit translates a virtual address into a physical address.

Accordingly, Watkins does not need Hansen's virtual memory system that translates a task specific virtual address into a generalized virtual address, and translates the generalized virtual address into a physical address.

Moreover, as discussed above, the incorporation of the Hansen's system into the Watkins' system would not "allow multiple programs to simultaneously share a computer system's main memory," as the Examiner asserts.

In addition, the Examiner offered no logical reason, and no such reason is apparent, to support the conclusion that the proposed combination would "increase the overall efficiency and flexibility of the system."

Accordingly, the Examiner has failed to provide the requisite reasons for combining the references and thus to establish a *prima facie* case of obviousness.

Moreover, as the combination of Watkins with Hansen does not disclose the alternate access circuitry recited in claim 1, this combination cannot teach or suggest:

-the alternate access circuitry configured to perform writing data into the storage element in response to a first address signal supplied from the host interface to access the first register, when the system operates with the first type of software, as claim 2 requires;

-the alternate access circuitry configured to perform writing data into the storage element in response to a second address signal supplied from the host interface to access the second register, when the system operates with the second type of software, as claim 3 requires;

-the alternate access circuitry configured to perform reading data from the storage element in response to a first address signal supplied from the host interface to access the first register, when the system operates with the first type of software, and configured to perform reading data from the storage

element in response to a second address signal supplied from the host interface to access the second register, when the system operates with the second type of software, as claims 4 and 5 recite.

Further, the applied combination does not teach or suggest the specific writing arrangements in the alternate access circuitry recited in claims 6-10. It is submitted that the Examiner has failed to point out specifically wherein the references disclose these arrangements.

Moreover, the references do not teach or suggest the reading arrangements in the alternate access circuitry recited in claims 11-13.

It is noted that the Examiner relies upon col. 9, lines 10-24 of Hansen for disclosing the subject matter of claims 2-5, and upon col. 4, lines 45-57 and col. 9, lines 10-24 of Hansen for disclosing the subject matter of claims 11-13.

It is respectfully submitted that the relied paragraphs of the reference do not disclose the claimed subject matter.

Claims 15-17

Independent claim 15 recites a network interface comprising:

- a host interface for supplying address, data and control signals from a host,

- storage element for holding a data element accessible via the host interface, and

- alternate access circuitry coupled to the storage element for providing multiple paths for accessing the data element, and configured to select a path for accessing the data element depending on a type of software used to operate the network interface.

The Examiner contends that Watkins discloses alternate access circuitry coupled to the storage element for providing multiple paths for accessing the data element. However, the Examiner admits that Watkins does not disclose selecting a path for accessing the data element depending on a type of software used to operate the network interface.

Hansen is relied upon for disclosing selecting a path for accessing the data element depending on a type of software used to operate the network interface. However, none of the paragraphs of Hansen relied upon by the Examiner teaches or suggests selecting a path for accessing the same data element depending on a type of software used to operate the network interface.

Moreover, it is noted that Hansen does not disclose selecting a path for accessing the same data element depending on threads.

Accordingly, a combination of the references would not teach or suggest the claimed alternate access circuitry coupled to the storage element for providing multiple paths for accessing the same data element, and configured to select a path for accessing the same data element depending on a type of software used to operate the network interface, as claim 15 requires.

Further, the references neither teach nor suggest the path for accessing the data element allocated in response to an address signal supplied from the network interface to access a

predetermined register, when a selected type of software is used to operate the network interface, wherein the selected type of software requires the data element to be held in the predetermined register, as claims 16 and 17 recite.

It is respectfully submitted that the paragraphs of Hansen relied upon by the Examiner for disclosing the subject matter of claims 16 and 17, do not teach or suggest this subject matter.

Claims 18-20

Independent claim 18 recites a method of providing access to a storage element for holding a data element, comprising the steps of:

- accessing the data element via a first access path when a first type of software is used to operate the data processing system, and

- accessing the data element via a second access path when a second type of software is used to operate the data processing system.

The Examiner has failed to address the steps recited in claim 18. However, as demonstrated above, neither Watkins nor Hansen discloses accessing the data element via a first access path when a first type of software is used to operate the data processing system, and accessing the same data element via a second access path when a second type of software is used to operate the data processing system. Accordingly, the reference combination is not sufficient to arrive at the invention of claim 18.

Moreover, the references do not teach or suggest that the first access path is allocated in response to a first address signal identifying a first register required by the first type of software to hold the data element, and the second access path is allocated in response to a second address signal identifying a second register required by the second type of software to hold the data element, as claims 19 and 20 recite.

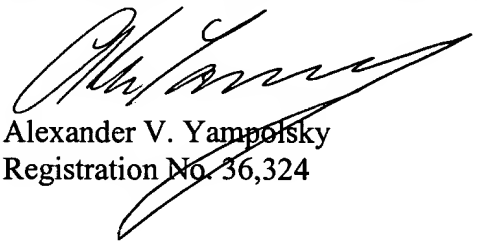
It is respectfully submitted that the paragraphs of Hansen relied upon by the Examiner for disclosing the subject matter of claims 19 and 20 do not teach or suggest this subject matter.

Conclusion

For the reasons advanced above, appellant respectfully contends that the rejection of claims 1-13 and 15-20 as being obvious under 35 U.S.C. § 103 is improper as the Examiner has not met the burden of establishing a *prima facie* case of obviousness. Reversal of the rejection in this appeal is respectfully requested.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP



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CLAIMS APPENDIX

1. A data processing system operable with at least two types of software, the system comprising:

a host interface for providing address, data and control signals from a host,

a storage element for holding data accessible via the host interface, and

alternate access circuitry for providing access to the storage element so as to access the data as a first data element in a first register when the system operates with a first type of software, and as a second data element in a second register when the system operates with a second type of software.

2. The system of claim 1, wherein the alternate access circuitry is configured to perform writing data into the storage element in response to a first address signal supplied from the host interface to access the first register, when the system operates with the first type of software.

3. The system of claim 2, wherein the alternate access circuitry is configured to perform writing data into the storage element in response to a second address signal supplied from the host interface to access the second register, when the system operates with the second type of software.

4. The system of claim 1, wherein the alternate access circuitry is configured to perform reading data from the storage element in response to a first address signal supplied from the host interface to access the first register, when the system operates with the first type of software.

5. The system of claim 4, wherein the alternate access circuitry is configured to perform reading data from the storage element in response to a second address signal supplied from the host interface to access the second register, when the system operates with the second type of software.

6. The system of claim 1, wherein the alternate access circuitry comprises a writing multiplexer having a first input for supplying the first data element to the storage element when the system operates with the first type of software, and a second input for supplying the second data element to the storage element when the system operates with the second type of software.

7. The system of claim 6, wherein the writing multiplexer is controlled by a first select signal to pass the first data element to the storage element when the first select signal is asserted.

8. The system of claim 7, wherein the writing multiplexer is controlled by a second select signal to pass the second data element to the storage element when the second select signal is asserted.

9. The system of claim 8, wherein the first select signal is asserted in response to a first address signal supplied from the host interface to access the first register.

10. The system of claim 9, wherein the second select signal is asserted in response to a second address signal supplied from the host interface to access the second register.

11. The system of claim 1, wherein the alternate access circuitry comprises a first reading gate coupled to the storage element for outputting the first data element when the system operates with the first type of software, and a second reading gate coupled to the storage element for outputting the second data element when the system operates with the second type of software.

12. The system of claim 11, wherein the first reading gate is configured to output the first data element in response to a first address signal supplied from the host interface to access the first register.

13. The system of claim 12, wherein the second reading gate is configured to output the second data element in response to a second address signal supplied from the host interface to access the second register.

Claim 14 (cancelled)

15. A network interface comprising:

a host interface for supplying address, data and control signals from a host,

a storage element for holding a data element accessible via the host interface, and

alternate access circuitry coupled to the storage element for providing multiple paths for accessing the data element, and configured to select a path for accessing the data element depending on a type of software used to operate the network interface.

16. The network interface of claim 15, wherein the path for accessing the data element is allocated in response to an address signal supplied from the network interface to access a predetermined register, when a selected type of software is used to operate the network interface.

17. The network interface of claim 16, wherein the selected type of software requires the data element to be held in the predetermined register.

18. In a data processing system, a method of providing access to a storage element for holding a data element, comprising the steps of:

accessing the data element via a first access path when a first type of software is used to operate the data processing system, and

accessing the data element via a second access path when a second type of software is used to operate the data processing system.

19. The method of claim 18, wherein the first access path is allocated in response to a first address signal identifying a first register required by the first type of software to hold the data element.

20. The method of claim 19, wherein the second access path is allocated in response to a second address signal identifying a second register required by the second type of software to hold the data element.